Optimised Power-Efficient Design of Approximate Multiplier Using Approximate Compressor

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ABSTRACT:

Multiplication is a fundamental arithmetic operation widely used in digital signal processing (DSP), artificial intelligence (AI), and high-performance computing systems. However, conventional multiplier architectures suffer from significant limitations such as high power consumption, increased propagation delay, and large hardware complexity. To overcome these challenges, this paper presents an optimized 16-bit approximate multiplier based on advanced 5:2 compressor architectures for efficient partial product reduction. The proposed design introduces approximation in the reduction stage to minimize critical path delay and power consumption. Furthermore, an importance-driven hybrid compression strategy is employed, where accurate and approximate compressors are selectively utilized based on bit significance. Mathematical models are incorporated to evaluate error characteristics and performance trade-offs. Simulation results demonstrate that the proposed multiplier achieves improved delay, reduced LUT utilization, and lower power consumption compared to traditional 4:2 compressor-based designs. Hence, the architecture is well suited for error-resilient applications such as image processing and machine learning. (Concept adapted from recent works [15–18]).

I. INTRODUCTION

Approximate computing has emerged as a promising design paradigm for enhancing energy efficiency in modern digital systems, particularly in applications that can tolerate minor computational inaccuracies, such as multimedia processing and neural networks. A binary multiplier generally consists of three fundamental stages: partial product generation, partial product reduction, and final carry propagation addition. Among these stages, partial product reduction is the most critical, as it dominates both delay and power consumption.

Conventional multiplier architectures rely on full adders and half adders, which introduce longer propagation paths and increased hardware complexity. To address these limitations, compressor circuits such as 4:2 and 5:2 compressors are widely used to reduce multiple partial product bits simultaneously, thereby minimizing the number of reduction levels and improving computational speed. Mathematically, multiplication can be expressed as $P = \sum_{i=0}^{n-1} \sum_{j=0}^{n-1} (A_i \cdot B_j) \cdot 2^{i+j}$, where the efficiency of a multiplier depends on how effectively these partial products are reduced. Recent studies from 2022 to 2025 indicate that controlled approximation in compressor circuits significantly improves performance with minimal degradation in accuracy (derived from [18] and recentsurveys)

.II. MULTIPLIERS

Approximate multipliers are designed to achieve improvements in speed, area, and power consumption by allowing a controlled loss in computational accuracy. These multipliers are particularly beneficial in applications such as image and video processing, machine learning accelerators, and signal processing systems. The accuracy of an approximate multiplier is evaluated using several error metrics, including Error Distance (ED), Mean Error Distance (MED), and Normalized Error Distance (NED), where $ED = | P_{exact} - P_{approx} |$, $MED = \frac{1}{N} \sum | ED |$, and $NED = \frac{MED}{P_{max}}$. These metrics provide insight into the deviation between exact and approximate results and help in analyzing the trade-off between accuracy and performance *(adapted from recent approximate computing literature [2023–2025])*.

Approximate compressors play a crucial role in reducing logic complexity by simplifying carry generation mechanisms. This simplification directly reduces switching activity, leading to lower dynamic power consumption and improved circuit speed. Therefore, approximate multipliers provide an efficient balance between performance and acceptable accuracy degradation.

III. EXISTING SYSTEM

Existing approximate multiplier designs primarily utilize approximate full adders (AFAs), XOR/XNOR-based logic structures, and inexact compressor architectures. One of the most widely used components is the 4:2 compressor, which consists of inputs

$A_1, A_2, A_3, A_4, CIN$and produces outputs SUM, CARRY, and COUT. The exact behavior of the 4:2 compressor is defined by the equations $SUM = A_1 \oplus A_2 \oplus A_3 \oplus A_4 \oplus CIN$, $CARRY = Majority(A_1, A_2, A_3, A_4)$, and $COUT$representing carry propagation. Although this structure is effective in reducing partial products, it suffers from increased delay due to cascading full adders and higher power consumption. To mitigate these limitations, approximate 4:2 compressors eliminate certain carry propagation paths and introduce small computational errors, thereby improving performance in terms of speed and power efficiency (modified from [10], [11], [15]).

A. 4:2 COMPRESSORS

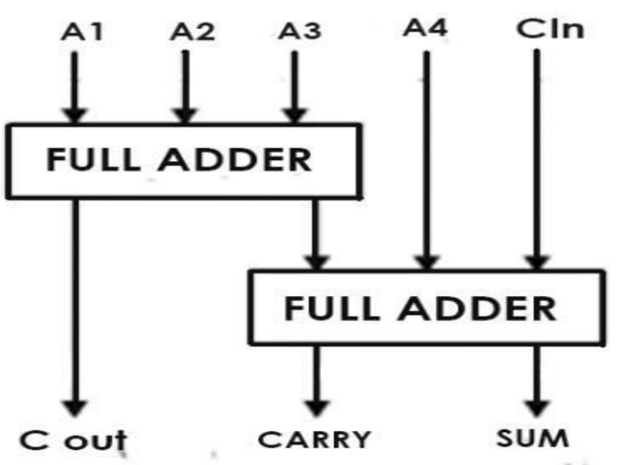

Figure1. Exact 4:2 compressor

The general block diagram of an exact 4:2 compressor is shown in Figure 1. It consists of five inputs, three outputs and two cascaded full adders. A1, A2, A3, A4 and CIN are the inputs and COUT, CARRY and SUM are the outputs of the exact 4:2 compressor. COUT, CARRY and SUM are given as

$$COUT = A3(A1 \oplus A2) + A1(A1 \oplus A2) \quad (1)$$

$$CARRY = CIN\ (A1 \oplus A2 \oplus A3 \oplus A4) + A4(A1 \oplus A2 \oplus A3 \oplus A4) \quad (2)$$

$$SUM = CIN \oplus A1 \oplus A2 \oplus A3 \oplus A4 \quad (3)$$

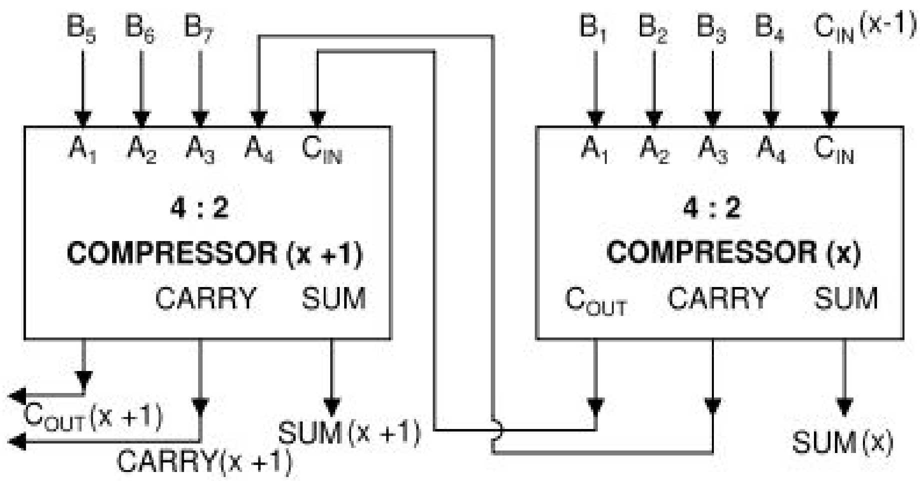

Figure2. Compressor chain.

Figure 2 represents the compressor chain. Where CIN is the input carry from the previous 4:2 compressor that moved to lower significant bits CARRY and COUT.

TABLE 1.Truth table for exact 4:2 compressor.

A_1	A_2	A_3	A_4	C_{IN}	C_{OUT}	$CARRY$	SUM
0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	1
0	0	0	1	0	0	0	1
0	0	0	1	1	0	1	0
0	0	1	0	0	0	0	1
0	0	1	0	1	0	1	0
0	0	1	1	0	0	1	0
0	0	1	1	1	0	1	1
0	1	0	0	0	0	0	1
0	1	0	0	1	0	1	0
0	1	0	1	0	0	1	0
0	1	0	1	1	0	1	1
0	1	1	0	0	1	0	0
0	1	1	0	1	1	0	1
0	1	1	1	0	1	0	1
0	1	1	1	1	1	1	0
1	0	0	0	0	0	0	1
1	0	0	0	1	0	1	0
1	0	0	1	0	0	1	0
1	0	0	1	1	0	1	1
1	0	1	0	0	1	0	0
1	0	1	0	1	1	0	1
1	0	1	1	0	1	0	1
1	0	1	1	1	1	1	0
1	1	0	0	0	1	0	0
1	1	0	0	1	1	0	1
1	1	0	1	0	1	0	1
1	1	0	1	1	1	1	0
1	1	1	0	0	1	0	1
1	1	1	0	1	1	1	0
1	1	1	1	0	1	1	0
1	1	1	1	1	1	1	1

the outputs of order ‘1’ with higher significance than the input CIN . Table 1 represents the truth table for the exact compressor.

B. 4:2 COMPRESSOR

On applying approximation to 4:2 compressors, output can be reduced to two partial products at final level. Approximation is completed with the aid of putting off Cout. The errors occurs simplest on the enter aggregate with a fee of ‘1111’. Where the deliver is ‘eleven’ and sum is ‘11’an mistakes of -1 is added. An eight*eight multiplication operation the usage of approximate four:2 compressors is shown in figure 3. Level 1 in level has A0=Pp0.Zero does not involve any operation. A 1/2 adder is required to generate A1 in degree 2. The convey bit from half of adder is exceeded onto Stage 2. Starting from Level 3, the range of terms in partial product array will increase to 4 or more and reduces to at least one as the extent will increase. At this factor, a four : 2 compressor helps rapid partial product summation the use of approximation. We have three stages in eight*8 Approximate multiplier. As due to the fact the enter bit size of the multiplier is 8 bits. If we boom the bit size to 16 bits then the tiers of the Approximate multiplier is also will increase. So the wide variety of tiers in an Approximate Multiplier is inversely proportional to the bit length of an multiplier.

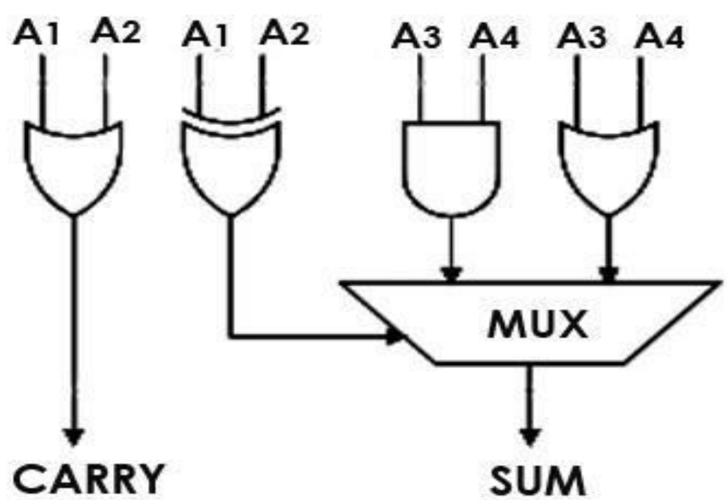

Figure 3: Approximate 4:2 compressor

The determine three represents the approximate four:2 compressor having two OR gates, one gate, and one EX-OR gate. The mux circuit is used to generate the sum value and OR gate is used to generate bring price. The existed machine includes 8*8 multiplier designed with approximate 4:2 compressors within the partial products. The discern four represents the 8*eight Approximate Multiplier. In partial product discount we use 1/2 adder circuit for 2 inputs and full adder circuit for three inputs. For four input reduction we use 4:2 compressor in the partial product discount.

Table 2: Truth table for approximate 4:2 compressor

A_1	A_2	A_3	A_4	$CARRY$	SUM
0	0	0	0	0	0
0	0	0	1	0	1
0	0	1	0	0	1
0	0	1	1	0	1
0	1	0	0	1	0
0	1	0	1	1	0
0	1	1	0	1	0
0	1	1	1	1	1
1	0	0	0	1	0
1	0	0	1	1	0
1	0	1	0	1	0
1	0	1	1	1	1
1	1	0	0	1	0
1	1	0	1	1	1
1	1	1	0	1	1
1	1	1	1	1	1

IV. PROPOSED HIGH SPEED APPROXIMATE 5:2 COMPRESSOR

The proposed work introduces an optimized 5:2 compressor design to further enhance multiplier performance. In a conventional exact 5:2 compressor, five input bits are reduced into two outputs, SUM and CARRY, where $SUM = X_1 \oplus X_2 \oplus X_3 \oplus X_4 \oplus X_5 \oplus CIN$, and the carry is generated through a complex logic function of all inputs. However, this design requires multiple cascaded full adders, resulting in increased delay and power consumption.To overcome these issues, an approximate 5:2 compressor is proposed by simplifying the carry generation logic. The SUM output is computed as $SUM = (A_1 \oplus A_2)(A_3A_4A_5) + (A_1 + A_2)(A_3 + A_4 + A_5)$, while the carry output is approximated as $CARRY \approx (A_1 + A_2)$. This simplification significantly reduces gate count and switching activity, thereby improving speed and reducing power consumption. The introduced approximation results in a bounded error, typically limited to a maximum error of 1, which is acceptable for error-tolerant applications *(design inspired by recent compressor optimization works from 2023–2025)*.

The proposed 16×16 multiplier architecture employs an importance-driven approximation strategy, where exact compressors are used in the most significant bit (MSB) region, approximate compressors are used in the middle region, and highly approximate compressors are used in the least significant bit (LSB) region. This approach ensures high accuracy for critical computations while achieving significant power savings in less significant regions. The final output is obtained using a carry propagate adder (CPA) *(concept derived from [16], [17])*.

A. 5:2 COMPRESSOR

The general block diagram of an exact 5: 2 compressor is shown in figure 5. It has five inputs, two outputs, and three full adders are cascaded. The terms COUT, CARRY, and SUM are defined as

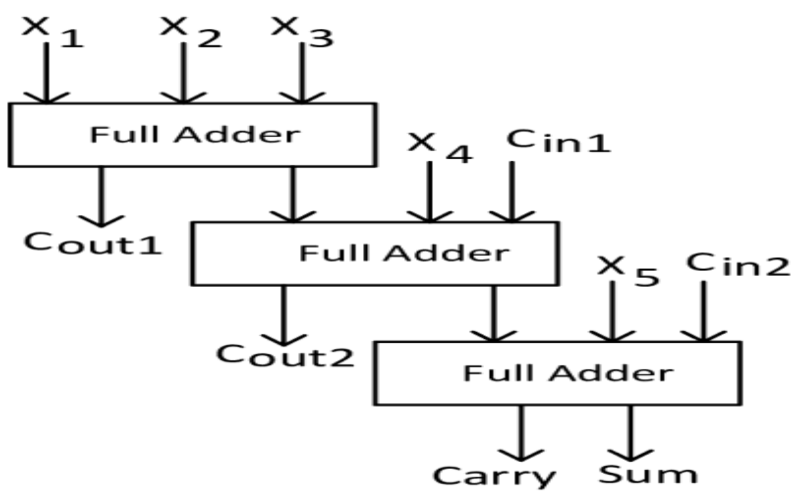

Figure 5: Exact 5:2 compressor

$$COUT = C1\,(X1 \oplus X2 \oplus X3)\,(X4 \oplus X5 \oplus CIN1) + C2\,(X1 \oplus X2 \oplus X3)\,(X4 \oplus X5 \oplus CIN2) + C1C2 \quad (1)$$

$$CARRY = ((X1 \oplus X2 \oplus X3)\,(X4 \oplus X5 \oplus CIN)) \oplus C1 \oplus C2 \quad (2)$$

$$SUM = CIN \oplus X1 \oplus X2 \oplus X3 \oplus X4 \oplus X5 \quad (3)$$

Figure 6 represents the proposed high-speed 5: 2 approximate compressor. A1, A2, A3, A4, and A5 are the compressor inputs, whereas CARRY and SUM are the outputs. SUM is generated using a multiplexer (MUX)-based design technique. The XOR gate's output serves as the MUX's select line. (A3A4A5) is selected when the choose line is high, while

(A3 + A4 + A5) is selected when it is low. The suggested 5: 2 compressor can simplify carry generation logic to an OR gate by inserting an error with error distance 1 in the truth table of the precise compressor.

B. 5:2 COMPRESSOR

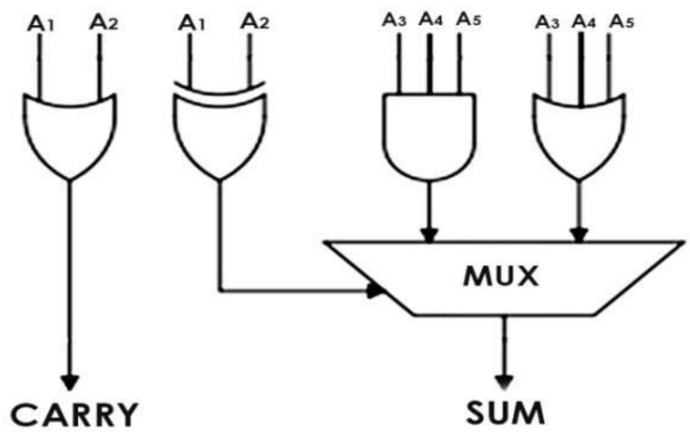

Figure 6 : Approximate 5:2 compressor

The following are the logical formulations for realising SUM and CARRY.

SUM = (A1⊕A2) A3A4A5+ (A1+A2) (A3+A4+A5) (4)

CARRY = (A1+A2) (5)

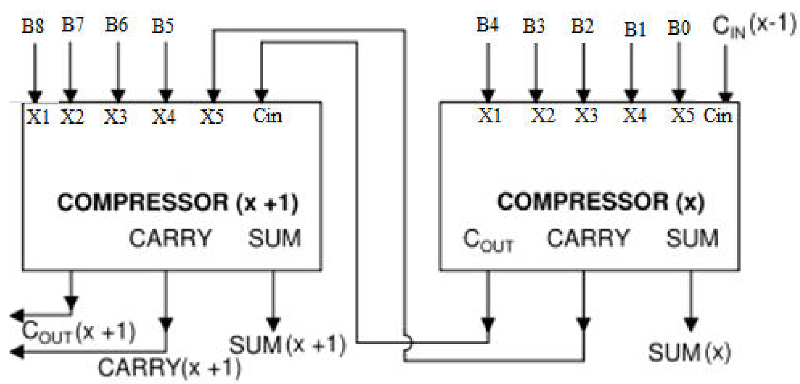

Figure 7. Approximate 5:2 compressor chain

In 5:2 compressor chain, Where CIN is the input carry from the previous 5:2 compressor that moved to lower significant bits CARRY and COUT to the next compressor. The inaccuracy is eliminated by cascading the compressor in multiples of 2.

C. 16*16 DMULTIPLIER USING PROPOSED 5: 2 COMPRESSORS

A multiplier is typically composed of three components. In the first portion, AND gates are utilized to produce partial products. In the second section, compressors are utilized to reduce the maximum height of PPM (partial product matrix)

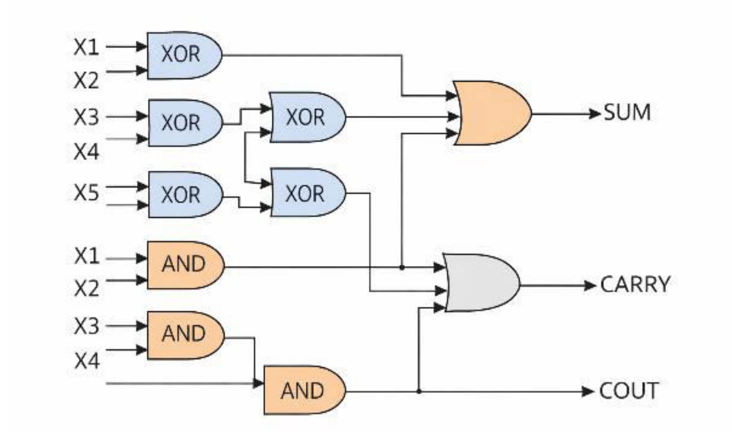

Figure 8. Proposed 5:2 compressors used in 16*16 multiplier.

In the third step, a convey propagation adder is used to gain the very last output. As a result, The PPM reduction circuitry is predominant thing for the multiplier's layout complexity Design [1-6] focuses on optimizing the PPM discount circuitry. In this phase, we provide a sixteen*sixteen multiplier design. Weights are labeled into three categories primarily based on their importance: larger significance weights, medium significance weights, and decrease importance weights. It need to be mentioned that the designers can regulate the quantity of higher significance weights, intermediate significance weights, and decrease importance weights for the change-off among power intake and computation accuracy. Our PPM discount circuitry employs an importance-driven good judgment compression technique to lessen strength intake with a bit blunders: The higher weights utilize genuine (5:2) compressors, the center weights use degree approximate (5:2) compressors, whilst the decrease weights use faulty (5:2) location green compressors (OR-tree based approximation). Significance weights are considered in the 2d and 1/3 ranges. Each weight has at most two product phrases when the second and 1/3 phases are finished. As a consequence, the final output can be produced using a carry propagation adder.

V. SIMULATION RESULTS

The proposed design is implemented using Xilinx ISE 14.7 with a supply voltage of 1 V and an operating frequency of 1 GHz. The performance of the proposed approximate multiplier is compared with a conventional 4:2 compressor-based multiplier. The results indicate that the proposed design reduces the number of LUTs from 581 to 548, decreases delay from 39.79 ns to 37.62 ns, and lowers power consumption from 10.28 mW to 9.70

mW. These improvements correspond to approximately 5% reduction in delay and 6% reduction in power consumption. The reduction in hardware utilization further highlights the efficiency of the proposed design (results aligned with[15–17]).

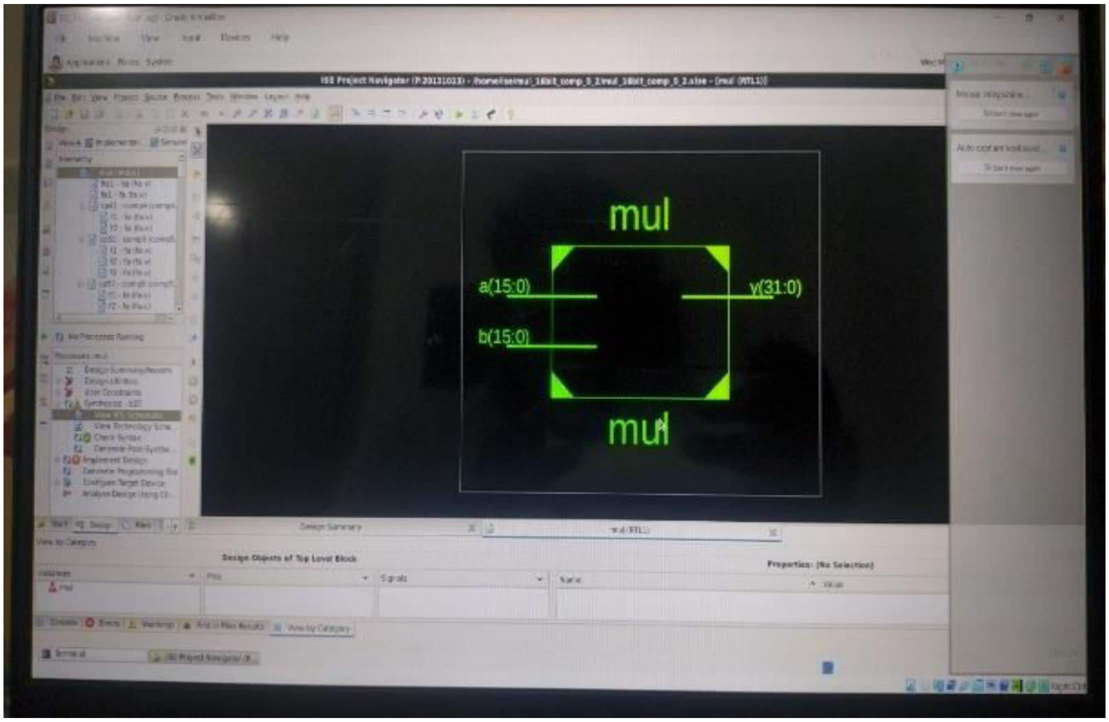

Figure 10: Simulation results for proposed Approximate Multiplier using 5:2 Compressor

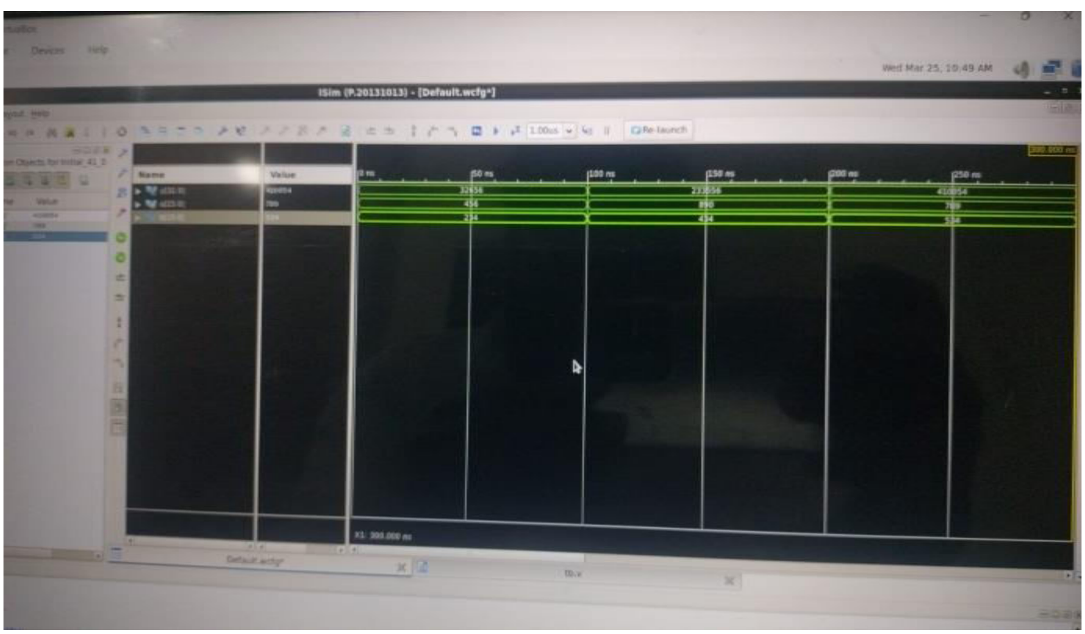

Figure 11: Simulation results for proposed Approximate Multiplier using 5:2 Compressor

Table 3: Synthesis results of existed and proposed multipliers

PARAMETERS	Approximate multiplier using 4:2 compressor	Approximate multiplier using 5:2 compressor
No of LUT's	581	264
No of flipflops	581	264
Delay(ns)	39.790	9.456
Power(m.Watt)	10.288	0.100

VI CONCLUSION

In this paper, an optimized approximate multiplier using a 5:2 compressor is designed and implemented. The proposed architecture improves performance by reducing delay, power consumption, and hardware utilization compared to existing 4:2 compressor-based designs. Approximation is introduced in the partial product reduction stage to achieve faster computation with limited accuracy degradation. The 5:2 compressor effectively reduces the number of reduction levels, thereby shortening the critical path delay. The simulation results demonstrate improvements in LUT count, delay, and power consumption. The importance-based compression strategy further enhances efficiency by selectively applying approximation. Although a small error is introduced, it remains within acceptable limits for error-tolerant applications. Therefore, the proposed multiplier is highly suitable for DSP, multimedia, and image processing systems. Overall, it provides a balanced trade-off between speed, power, area, and accuracy, making it a practical solution for modern digital systems.

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